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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,276	03/20/2001	Michio Horiuchi	072-01	2361

7590 04/08/2003

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EXAMINER
OWENS, DOUGLAS W

ART UNIT	PAPER NUMBER
2811	11

DATE MAILED: 04/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/812,276	Applicant(s) HORIUCHI ET AL.	
	Examiner Douglas W Owens	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-22,27 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-22,27 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 28, 2003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 20 – 22 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 5,892,271 to Takeda et al. in view of US patent No. 5,999,413 to Ohuchi et al.

Regarding claims 20 and 39, Takeda et al. teaches a semiconductor device, comprising:

a resin member of a predetermined thickness (19), said resin member being made of a seal resin (Col. 7, lines 9 – 13);

a semiconductor element (1) having an active surface facing downward;

metal interconnections (in via (14), see Col. 6, line 65 – Col. 7, line 2) formed directly on the bottom surface of the resin member; and

connection terminals (2, 3) extending downward from the active surface of the semiconductor element and having bottom ends connected to top surfaces of said metal interconnections (See for example, the connections in Fig. 8).

Takeda et al. further teaches a resin coating over the bottom side of the semiconductor element to seal the electrode surface of the element inside the coating (Col. 7, lines 9-13) so that the back surface of the chip is exposed. Takeda et al. does not teach resin on the sides of the chip, such that the chip is enclosed.

Ohuchi et al. teaches a semiconductor device wherein the semiconductor element (21) is sealed inside the resin member (26) and wherein the element has a back surface exposed at a top surface of the resin member (Fig. 4, for example), the surface of the resin and semiconductor element being in the same plane. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Ohuchi et al. into the device taught by Takeda et al. since it is desirable to protect the chip from the detrimental effects of the environment, such as moisture and debris.

Regarding claim 21, the combined teaching of Takeda et al. and Ohuchi et al. disclose a device wherein the back surface of the semiconductor element and the top surface of the resin member form the same plane.

Regarding claim 22, the proposed device of Takeda et al. and Ohuchi et al. discloses a semiconductor device, as recited above, further disclosing wherein the

device is provided with a solder resist layer covering the entire bottom surface of said resin member including said metal interconnections, passing through said solder resist layer, and projecting downward (see, for example, Takeda et al., Fig. 8 (15) and Col. 7, lines 13-17).

4. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al. and Ohuchi et al. as applied to claim 20 above, and further in view of US patent No. 6,023,096 to Hotta et al.

Neither Takeda et al. nor Tomikawa et al. teach a device, wherein an inorganic filler is dispersed in the resin member. Hotta et al. teaches a semiconductor device, wherein an inorganic filler is dispersed in the resin member (Col. 5, lines 54-65). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Hotta et al. into the device taught by Takeda et al. and Ohuchi et al. since it is desirable to protect the chip from the effects of differential thermal expansion.

Response to Arguments

5. Applicant's arguments with respect to claims 20 – 22 and 27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for

the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DWO
April 2, 2003